



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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EWm  
3-16-04

In re Patent Application of:

Louzoun

Application No.: 10/082,434

Filed: February 22, 2002

For:

**SYSTEM AND METHOD FOR EFFICIENT  
SCHEDULING OF MEMORY**

Examiner: Truong, Bao Q..

Art Unit: 2187

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**MAR 12 2004**

Technology Center 2100

**AMENDMENT**

ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

Dear Sir:

In response to the Office Action, dated November 3, 2003, please make the  
following amendments and consider the following remarks:

1.(currently amended) A method comprising:

receiving a plurality of commands to access at least one of a plurality of memory

banks of a memory; and

scheduling the plurality of commands based at least in part on a status

information of at least one of the plurality of memory banks; and

arbitrating between the commands to determine priority of access to the memory bus

based at least in part on the status information

2. (original) The method of claim 1 wherein the memory is a synchronous dynamic

random access memory.

1 3. (original) The method of claim 1 wherein the status information based at least in part  
2 on an idle state of the plurality of memory banks with respect to a bank based queuing  
3 scheme.

1 4. (original) The method of claim 1 wherein the status information is either an idle state  
2 of the plurality of memory banks.

A, 1 5. (original) The method of claim 1 wherein the status information is based at least in  
2 part on a type of a most\_recent command forwarded to the memory device via a  
3 memory bus.

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5 6. (original) The method of claim 1 wherein the plurality of commands are read and  
6 write commands.

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16 7. (currently amended) A system comprising:  
17 a processor; and  
18 a logic, coupled to the processor and to at least one memory device with a  
19 plurality of memory banks, to receive commands to access the memory  
20 device  
21 and to schedule and arbitrate the commands based at least in part on a  
22 status information of the plurality of memory banks.

A<sub>1</sub>

1 8. (original) The system of claim 7 wherein the commands are read and write  
2 commands.

1 9. (original) The system of claim 7 wherein the wherein the status information is based  
2 at least in part on a type of most recent command forwarded to the memory device via  
3 a memory bus.

1 10. (original) The system of claim 7 wherein the plurality of memory banks perform in  
2 parallel.

3  
1 11. (original)\_ The system of claim 7 wherein the logic is a network switch or a  
2 memory controller.

1 12. (original)\_ The system of claim 7 wherein the status information is an idle state of  
2 the plurality of memory banks.

3

4 13. (original) The system of claim 7 wherein the memory is a synchronous dynamic  
5 random access memory.

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2 14. (currently amended) An apparatus comprising:

3 a first logic, coupled to at least one memory device with a plurality of memory  
4 banks, to receive commands to access the memory device; and  
A, 5 a second logic, coupled to the first logic, to schedule and arbitrate the received  
6 commands based at least in part on a status information of the plurality of  
7 memory banks.

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9 15. (original) The apparatus of claim 14 further comprising a third logic to forward the  
10 schedule of the received commands to the memory device via a memory bus.

11

12 16. (original) The apparatus of claim 14 wherein the apparatus is either one of a  
13 network switch or memory controller.

14

15 17. (original) The apparatus of claim 14 wherein the memory device is a synchronous  
16 dynamic random access memory.

17

18 18. (original) The apparatus of claim 14 wherein the received commands are read  
19 and write commands.

20

21 | 19. (original)\_ The apparatus of claim 14 wherein the status information is based at least  
22 | in part on a type of most recent command forwarded to the memory device via the  
23 | memory bus.

24

25 | 20. (original)\_ The apparatus of claim 14 wherein the plurality of memory banks perform  
26 | in parallel.

27

A | 28 | 21. (original)\_ The apparatus of claim 14 wherein the status information is an idle state  
29 | of the plurality of memory banks.

30

31 | 22.\_(currently amended)A method comprising:

32 | receiving a plurality of commands to access at least one of a plurality of memory  
33 | banks of a memory coupled to a memory bus;

34 | scheduling the plurality of commands based at least in part on a status  
35 | information of at least one of the plurality of memory banks; and

36 | arbitrating between the commands to determine priority of access to the memory  
37 | bus based at least in part on the status information.

38

39 | 23. (original) The method of claim 22 wherein the memory is a synchronous dynamic  
40 | random access memory.

1 | 24.\_(original) The method of claim 22 wherein the status information is an idle state of  
2 | the plurality of memory banks.

1 | 25\_(original) The method of claim 22 wherein the plurality of memory banks perform in  
2 | parallel.

3 | 26. (original) The method of claim 22 wherein the status information is based at least in  
4 | part on a type of a most\_recent command forwarded to the memory device via a  
5 | memory bus.

6 |  
A | 7 | 27. (original)\_ The method of claim 22 wherein the plurality of commands are read and  
8 | write commands.

9 |  
10 | 28. \_(currently amended)\_An article comprising:

11 | a storage medium having stored thereon instructions, that, when executed by a  
12 | computing platform, result in forwarding a plurality of commands to a memory device by:

13 | receiving the plurality of commands to access at least one of a plurality of  
14 | memory banks of the memory device; and

15 | scheduling and arbitrating the plurality of commands based at least in part on a  
16 | status information of at least one of the plurality of memory banks.

17 |  
18 | 29\_(original) The article of claim 28 wherein the memory is a synchronous dynamic  
19 | random access memory.

1 | 30\_(original) The article of claim 28 wherein the status information is an idle state of  
2 | the plurality of memory banks.

1 | 31\_(original) The article of claim 28 wherein the plurality of memory banks perform in parallel.

2 | 32. (original) The article of claim 28 wherein the status information is based at least in part on

A | 3 | a type of a most\_recent command forwarded to the memory device via a memory bus.

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5 | 33. (original) The article of claim 28 wherein the plurality of commands are read and write

6 | commands.

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